AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application. Applicant by this Amendment, cancels claims 3 and 7-13, amends claims 1, 2, 4 and 5, and adds new claims 14-27. Claims 1-2, 4-6, and 14-27 are pending for consideration.

Listing of Claims:

1. (Currently Amended) A method for manufacturing a semiconductor device, comprising:

forming first spacers on sidewalls of first structures, wherein each one of the first structures ~~include~~ comprises; an insulation film pattern formed on a conductive film pattern ~~layers and insulation pattern layers stacked~~ formed on a semiconductor substrate, wherein ~~a thickness of each of~~ the conductive film pattern is formed with a thickness ~~insulation pattern layers is~~ at least four times that of the insulation film pattern~~thinner than a thickness of each of the conductive pattern layers~~;

forming a first insulation film to cover the first structures including the first spacers and regions between the first structures;

forming first insulation film patterns filling ~~pattern layers located in the~~ regions between adjacent ones of the first structures by planarizing the first insulation film until upper faces of the first structures are exposed;

forming second structures on the first insulation film patterns and on the first structures,

wherein each one of the second structures is substantially aligned over at least one of the first structures, such that the second structures expose first portions of the first insulation film patterns, wherein each one of the exposed first portions ~~are~~ is spaced from adjacent ones of the first structures by a distance ~~which is~~ ranging from

between about 5 to about 35 percent of ~~an interval~~ a distance separating the adjacent ones of ~~between~~ the first structures; and

forming openings ~~in the first insulation film which~~ to expose portions of the semiconductor substrate by etching the first portions of the first insulation film patterns using the second structures and the first spacers as an etching mask.

2. (Currently Amended) The method of claim 1, wherein formation of the second structures comprises:

forming an etch stop film on the first insulation film patterns and on the first structures;

forming etch stop film patterns which expose portions of the first insulation film patterns by etching the etch stop film;

uniformly forming a spacer film on the etch stop film patterns and on the exposed portions of the first insulation film patterns; and

forming second spacers on sidewalls of the etch stop film patterns by anisotropically etching the spacer film ~~so that the second structures including the etch stop film patterns and the second spacers are formed~~, wherein the second spacers are separated from adjacent ones of the first structures by a distance ~~which is~~ ranging from about 5 to about 35 percent of the ~~intervals between~~ distance separating the adjacent ones of the first structures.

3. (Canceled)

4. (Currently Amended) The method of claim 1, wherein formation of the second structures comprises:

forming an etch stop film on the first insulation film patterns and on the first structures;

forming photoresist patterns on the etch stop film ~~which are located over the film insulation film patterns~~ substantially edge aligned over the first structures;

forming the second structures ~~which extend~~ spaced apart from adjacent ones of the first structures by a distance ~~of~~ ranging from between about 5 to about 35 percent of the ~~intervals between~~ distance separating the adjacent ones of the first structures by etching the etch stop film using the photoresist patterns as etching masks; and

removing the photoresist patterns.

5. (Currently Amended) The method of claim 1, wherein forming the openings in the first insulation film pattern is performed using an etching process having an etching selectivity relative to the ~~in which each~~ first insulation film ~~pattern has an etching selectivity~~ of more than about 10:1 relative to ~~each~~ the second structures.~~structure and each first spacer.~~

6. (Original) The method of claim 1, wherein each second structure has a thickness which is less than that of the first structures.

Claims 7-13 (Canceled)

14. (New) A method for manufacturing a semiconductor device, comprising:

forming first spacers on sidewalls of first structures, wherein each one of the first structures comprises an insulation film pattern and a conductive film pattern stacked on a semiconductor substrate, wherein the conductive film pattern is formed with a thickness at least four times that of the insulation film pattern;

forming a first insulation film to cover the first structures including the first spacers and regions between the first structures;

forming first insulation film patterns filling regions between the first structures by planarizing the first insulation film until upper faces of the first structures are exposed;

forming second structures on the first insulation film patterns and on the first structures, such that the second structures expose first portions of the first insulation

film patterns, wherein each one of the exposed first portions is spaced from adjacent ones of the first structures by a distance ranging from between about 5 to about 35 percent of a distance separating the adjacent ones of the first structures;

forming openings to expose portions of the semiconductor substrate by etching the first portions of the first insulation film patterns using the second structures and the first spacers as an etching mask;

wherein formation of the second structures comprises;

forming an etch stop film on the first insulation film patterns and on the first structures;

forming hard mask patterns on the etch stop film, each one of the hard mask patterns being substantially aligned over at least one of the first structures;

forming second spacers on sidewalls of the hard mask patterns;

etching portions of the etch stop film using the hard mask patterns and the second spacers as an etching mask; and

removing the hard mask patterns and the second spacers.

15. (New) The method of claim 14, wherein the first insulation layer comprises at least one selected from a group consisting of; BPSG, a high density plasma (HDP) oxide, a high temperature undoped silicate glass (HTUSG), and a spin-on-dielectric (SOD) material.

16. (New) The method of claims 15, wherein forming the first insulation film patterns comprises planarizing the first insulation layer using at least one of a chemical mechanical polishing (CMP) process and an etch-back process.

17. (New) The method of claim 14, wherein adjacent ones of the hard mask patterns are separated by a distance greater than the distance separating the adjacent ones of the first structures.

18. (New) The method of claim 14, wherein forming the openings in the first insulation film comprises:

etching the first insulation film patterns using an etching process having an etching selectivity relative to the first insulation film patterns of more than about 10:1 relative to the hard mask patterns and second sidewalls.

19. (New) The method of claim 14, wherein the hard mask patterns are formed with a thickness less than that of the first structures.

20. (New) A method for manufacturing a semiconductor device, comprising:

forming first structures comprising a plurality of gate electrode structures, each one of the plurality of gate electrode structures comprising an insulation film pattern serving as an etch end point and formed on a conductive film pattern which is formed on a gate oxide film pattern, wherein the conductive film pattern is formed with a thickness at least four times that of the insulation film pattern, and wherein each one of the plurality of gate electrode structures is separated from adjacent ones of the plurality of gate electrode structures by a first distance;

forming first spacers on sidewalls of each one of the plurality of gate electrode structures;

forming a first insulation film on the plurality of gate electrode structures and first spacers;

forming first insulation film patterns completely filling regions between adjacent ones of the plurality of gate electrodes and their associated first spacers by planarizing the first insulation film using the etch stop point;

forming second structures on the first insulation film patterns, wherein each one of the second structures is substantially edge aligned with at least one of the first spacers, such that the second structures expose portions of the first insulation film

patterns having a width ranging from between about 5 to about 35 percent less than the first distance; and

forming openings to expose portions of the semiconductor substrate by etching the first portions of the first insulation film pattern using the second structures and the first spacers as an etching mask.

21. (New) The method of claim 20, wherein forming the second structures comprises:

forming an etch stop film on the first insulation film patterns and the first structures;

forming hard mask patterns to expose portions of the etch stop film having a width substantially equal to and overlaying the width of the exposed portions of the first insulation film patterns;

etching the etch stop film using the hard mask patterns as an etching mask; and,

removing the hard mask patterns.

22. (New) The method of claim 21, wherein forming the hard mask patterns comprises:

forming a hard mask film on the etch stop film;

patterning the hard mask film into hard mask portions substantially edge aligned with at least one gate electrode structure;

forming second spacers on sidewalls of the hard mask portions.

23. (New) The method of claim 21, wherein the first insulation layer comprises at least one selected from a group consisting of; BPSG, a high density plasma (HDP) oxide, a high temperature undoped silicate glass (HTUSG), and a spin-on-dielectric (SOD) material.

24. (New) The method of claims 23, wherein forming the first insulation film patterns comprises planarizing the first insulation layer using at least one of a chemical mechanical polishing (CMP) process and an etch-back process.

25. (New) The method of claim 21, wherein adjacent ones of the hard mask patterns are separated by a distance greater than the distance separating the adjacent ones of the first structures.

26. (New) The method of claim 24, wherein forming the openings in the first insulation film comprises:

etching the first insulation film patterns using an etching process having an etching selectivity relative to the first insulation film patterns of more than about 10:1 relative to the hard mask patterns and second sidewalls.

27. (New) The method of claim 21, wherein the hard mask patterns are formed with a thickness less than that of the first structures.